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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,994	07/28/2003	Thomas M. Graettinger	2003-0236.00/US	7334

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,994	GRAETTINGER ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on July 22nd, 2005. These drawings are approved.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 and 20-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Zheng et al. (U.S. Pub. 2003/0166318).

In re claim 1, **Zheng** discloses a method for forming a semiconductor device capacitor, comprising: providing a base dielectric layer **16** (page 1, paragraph [0012] and FIG. 1);

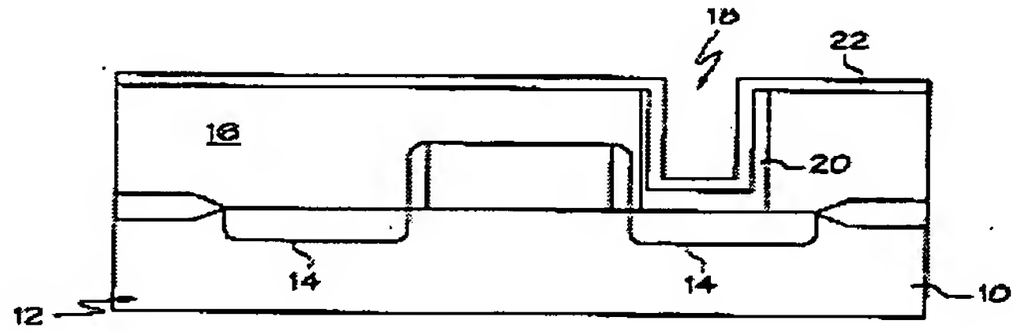

FIG. 1

etching the base dielectric layer to form an opening **18** therein, the opening defined by first and second cross-sectional dielectric sidewalls;

forming a first conductive cross-sectional spacer on the first dielectric sidewall wherein the first conductive spacer forms a portion of a capacitor top plate **20** (page 2, paragraph [0012]);

forming a first capacitor cell dielectric layer **22** on the first conductive spacer **20**; forming a second conductive cross-sectional spacer on the first capacitor cell dielectric layer;

forming a first conductive layer on the second conductive spacer, wherein the second conductive spacer and the conductive layer each form a portion of a capacitor bottom plate (page 1, paragraphs [0012]-[0014] and FIG. 2);

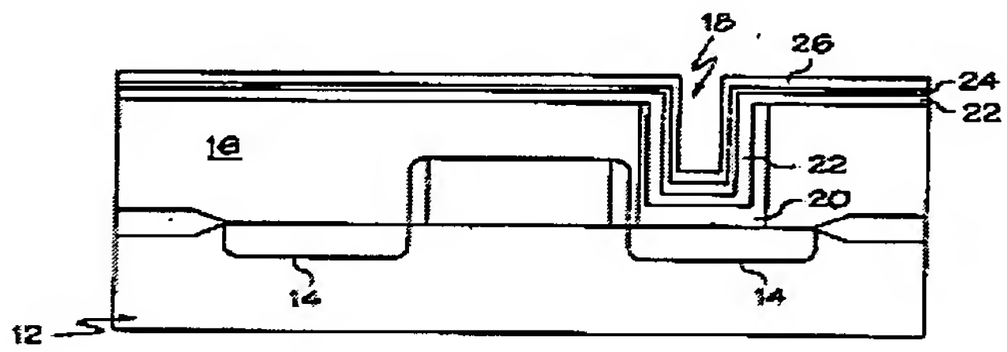

FIG. 2

forming a second cell dielectric layer on the first conductive layer;

forming a second conductive layer on the second cell dielectric layer, wherein the second conductive layer forms a portion of the capacitor top plate **26** ; and forming a conductive feature (unlabeled) which electrically connects the first conductive spacer and the second conductive layer (FIG. 3).

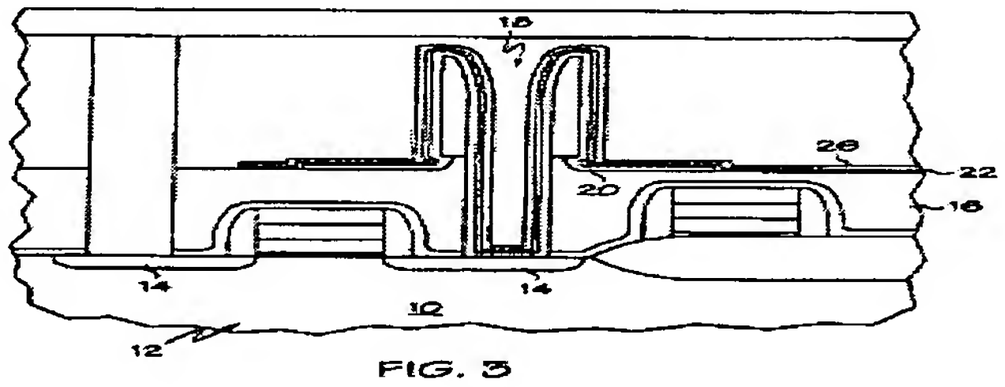

FIG. 3

In re claim 2, **Zheng** discloses that the method of claim 1, further comprising: prior to etching the base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer; during the etching of the base dielectric layer to form the opening, etching the third conductive layer to form an opening in the third conductive layer; forming said first conductive cross-sectional spacer to contact the third conductive layer; performing an etch which forms a cross-sectional third sidewall from the second conductive layer, the second cell dielectric layer, and the third conductive layer; and during the formation of said conductive feature: forming a conformal fourth conductive layer which contacts the second conductive layer and said third conductive layer; spacer etching the forth conductive layer which forms a third conductive cross-sectional spacer on the third sidewall and electrically connects the first conductive spacer and the second conductive layer through the third conductive layer (page 1, paragraph [0012] and FIGS. 1-2).

In re claim 3, **Zheng** discloses that the method of claim 2 further comprising forming fourth and fifth conductive cross-sectional spacers from said fourth conductive layer within said opening in said base dielectric layer during said spacer etch of said fourth conductive layer (page 1, paragraph [0012] and FIGS. 1-2).

In re claim 4, **Zheng** discloses that the method of claim 2 further comprising removing at least a portion of said third conductive layer using a planarizing process prior to forming said second cell dielectric layer (page 1, paragraph [0012] and FIGS. 1-2).

In re claim 5, **Zheng** discloses that the method of claim 4 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process (page 1, paragraph [0012] and FIGS. 1-2).

In re claim 6, **Zheng** discloses that the method of claim 1 further comprising: prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer; during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer; forming said first conductive cross-sectional spacer to contact said third conductive layer; etching said second conductive layer and said second cell dielectric layer to form an opening therein and to expose said third conductive layer; forming a conductive plug within said opening in said second conductive layer and said second cell dielectric layer, said plug contacting said second conductive layer and said third conductive layer to electrically connect said first conductive spacer and said second conductive layer through said third conductive layer (page 1, paragraph [0012] and FIGS. 1-2).

In re claim 7, **Zheng** discloses that the method of claim 6 further comprising removing at least a portion of said third conductive layer by a planarizing process prior to forming said second cell dielectric layer (page 1, paragraph [0012] and FIGS. 1-2).

In re claim 8, **Zheng** discloses that the method of claim 7 further comprising removing a portion of each of said first conductive cross-sectional

spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process (page 1, paragraphs [0012] and FIGS. 1-2).

In re claim 9, **Zheng** discloses a method used to form a semiconductor device, comprising: providing a semiconductor wafer substrate **12** assembly comprising a semiconductor wafer and a conductive contact pad overlying said wafer;

forming an etch stop layer on the contact pad; forming a blanket planarized base dielectric layer **16** on the etch stop layer; forming a conformal first conductive layer on the planarized base dielectric layer (page 1, paragraph [0012] and FIG. 1);

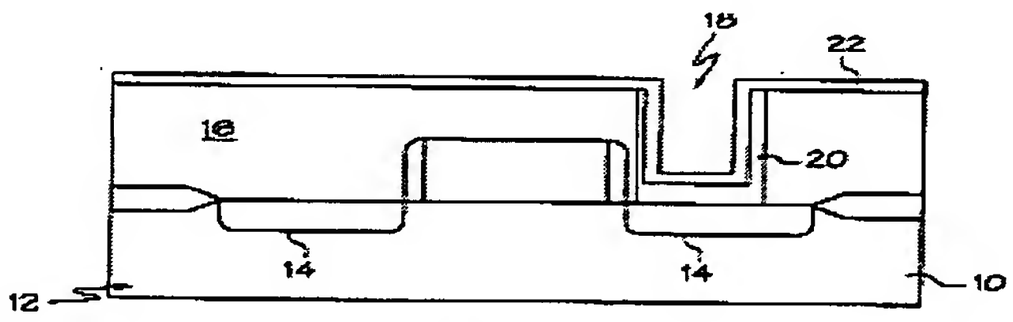

FIG. 1

etching the conformal first conductive layer and the planarized base dielectric layer to form first and second cross sectional sidewalls in the base dielectric layer which define a recess **18** in said the dielectric layer, wherein the etch exposes the etch stop layer; forming a second conductive layer which comprises a first conductive spacer **20** on the first sidewall (page 2, paragraph [0012]);

forming a first cell dielectric layer **22** on said first conductive spacer and on the etch stop layer; forming a third conductive layer **26** on the first cell

dielectric layer; spacer etching the third conductive layer and the first cell dielectric layer to form a second conductive spacer from the third conductive layer, to form a cell dielectric spacer from the first cell dielectric layer, and to expose said etch stop layer (page 1, paragraphs [0012]-[0014] and FIG. 2);

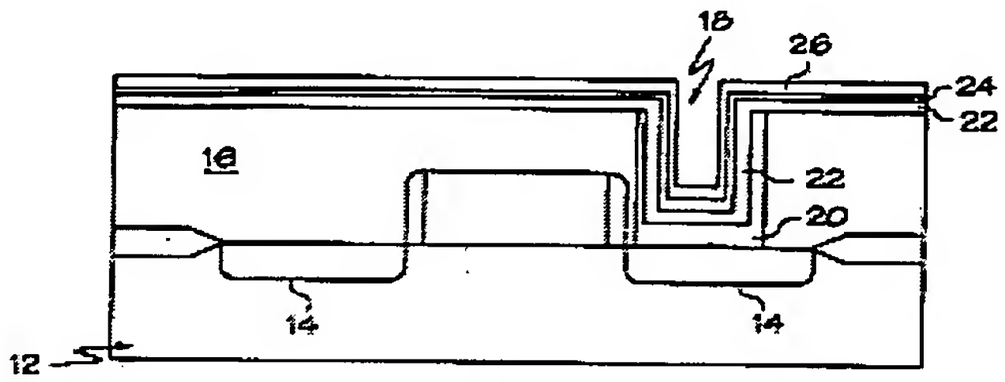

FIG. 2

subsequent to the spacer etching the third conductive layer and the first cell dielectric layer, etching the etch stop layer to expose the contact pad; forming a fourth conductive layer on the second conductive spacer and on the contact pad; forming a second cell dielectric layer on the fourth conductive layer; forming a fifth conductive layer on said second cell dielectric layer; and electrically connecting said first conductive spacer and said fifth conductive layer, wherein the second and fifth conductive layers form a first capacitor plate, and the third and fourth conductive layers form a second capacitor plate interposed between said first conductive spacer and said fifth conductive layer (page 1, paragraphs [0012]-[0014] and FIG. 3).

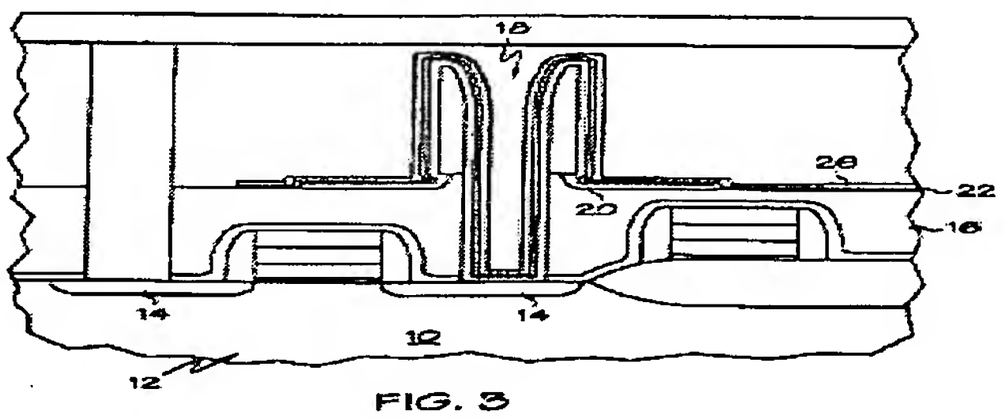

FIG. 3

In re claim 10, **Zheng** discloses that the method of claim 9 further comprising: during the formation of the second conductive layer, forming said spacer to contact said first conductive layer; etching an opening in said second cell dielectric layer and said fifth conductive layer to expose said first conductive layer; forming a conductive plug within said opening in said fifth conductive layer and said second cell dielectric layer, said plug contacting said first conductive layer and said fifth conductive layer to electrically connect said first conductive spacer and said fifth conductive layer through said first conductive layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 11, **Zheng** discloses that the method of claim 9 further comprising: performing an etch which forms a third cross-sectional sidewall from the fifth conductive layer, said second cell dielectric layer, and said first conductive layer; forming a sixth conductive layer over said fifth conductive layer and on said third cross-sectional sidewall; and spacer etching said sixth conductive layer to form a conductive spacer on said third cross-sectional sidewall which electrically connects said first conductive spacer and said fifth conductive layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 12, **Zheng** discloses that the method of claim 11 further comprising, during said formation of said sixth conductive layer, forming a portion of said sixth conductive layer within said opening in said base dielectric layer, wherein subsequent to spacer etching said sixth conductive layer, a portion of said sixth conductive layer remains in said opening in said base dielectric layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 20, **Zheng** discloses a method used to form a semiconductor device, comprising: forming a semiconductor wafer substrate assembly comprising a base supporting layer **16** having a recess **18** therein; within the recess in the base supporting layer, forming first and second conductive spacers **20** having a first cell dielectric **22** interposed therebetween which electrically isolates the first and second conductive spacers from each other; forming a first conductive layer electrically connected to the second conductive spacer within the recess (page 1, paragraph [0012] and FIG. 1);

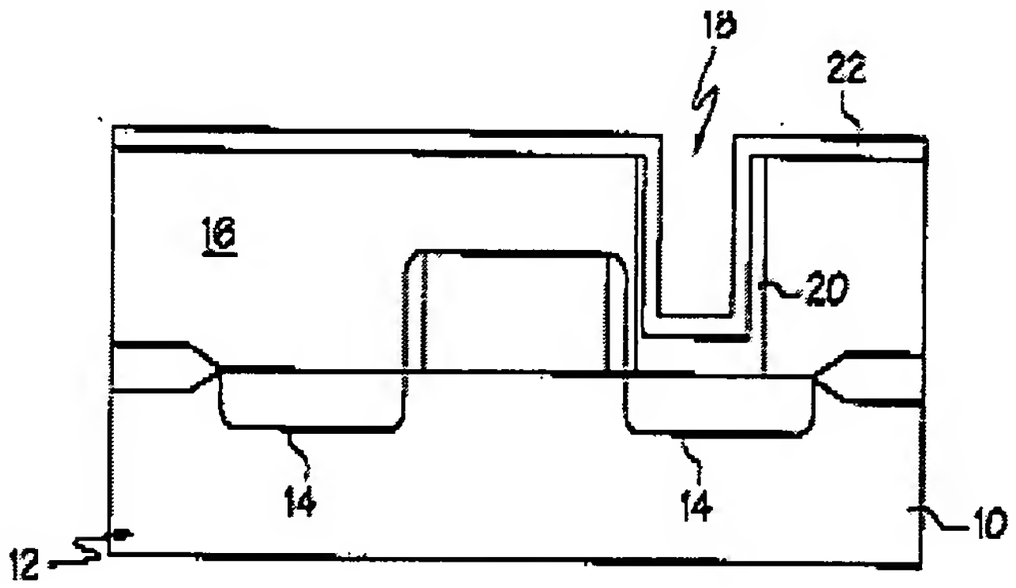

FIG. 1

forming a blanket second conductive layer over the first conductive layer and electrically separated from the first conductive layer by a second cell dielectric layer; and electrically connecting the first conductive spacer and the blanket second conductive layer to form a storage capacitor, where the first conductive spacer and blanket second conductive layer form a portion of a capacitor top plate **26** and the second conductive spacer and first conductive layer form a portion of a capacitor bottom plate 20 (page 1, paragraphs [0012]-[0014] and FIGS. 2-3).

In re claim 21, **Zheng** discloses that the method of claim 20 further comprising etching the blanket second conductive layer prior to electrically connecting the first conductive spacer and the blanket second conductive layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 22, **Zheng** discloses that the method of claim 21 further comprising: during the formation of the base supporting layer: forming a base dielectric layer and a base conductive layer over the base dielectric layer **16**; etching the base conductive layer and the base dielectric layer to form the recess **18** in the base supporting layer; and subsequent to the etching of the blanket second conductive layer, etching the base conductive layer to form a sidewall defined by the blanket second conductive layer and the base conductive layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 23, **Zheng** discloses that the method of claim 22 further comprising forming a third conductive spacer over the sidewall to electrically connect the blanket second conductive layer and the base conductive layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 24, **Zheng** discloses that the method of claim 22 further comprising: etching the blanket second conductive layer and the base conductive layer to form an opening therein; and forming a conductive plug within the opening to electrically connect the blanket second conductive layer and the base conductive layer (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 25, **Zheng** discloses a method used to form a semiconductor device comprising a storage capacitor having a top plate **26** and a bottom plate **20**,

comprising: forming a first portion of a capacitor top plate comprising a vertically-oriented conductive spacer; forming a first cell dielectric layer **22** to contact the first portion of the capacitor top plate **26** (page 1, paragraphs [0012]-[0014] and FIG. 1);

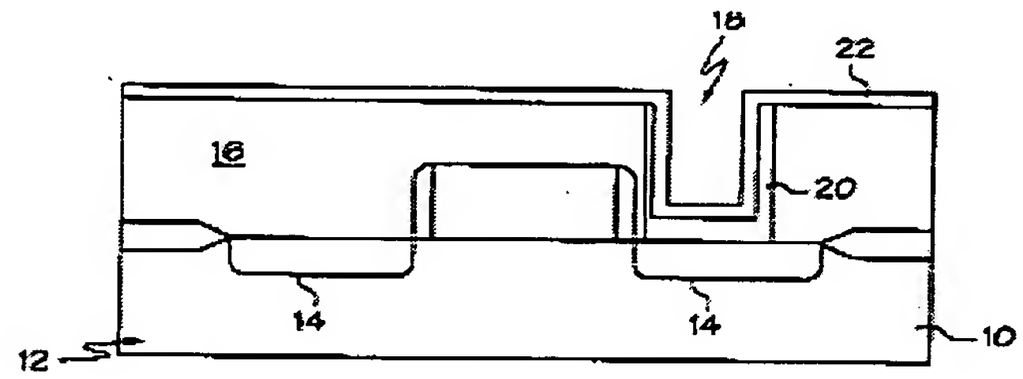

FIG. 1

forming a first portion of a capacitor bottom plate **20** comprising a vertically- oriented conductive spacer to contact the first cell dielectric layer;

forming a second portion of the capacitor bottom plate comprising a vertically-oriented layer to contact the first portion of the capacitor bottom plate **20**; forming a second cell dielectric layer to contact the second portion of the capacitor bottom plate (page 1, paragraphs [0012]-[0014] and FIG. 2);

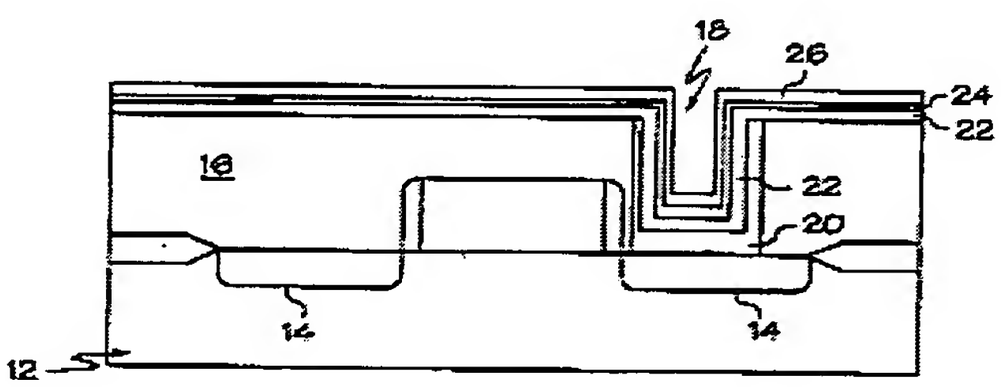

FIG. 2

forming a second portion of the capacitor top plate **26** to contact the second cell dielectric layer and which comprises a portion which overlies the first portion of the capacitor top plate, the first and second cell dielectric layers, and the first and second portions of the capacitor bottom plate; and forming a

conductive structure which electrically connects the first and second capacitor top plate portions (page 1, paragraphs [0012]-[0014] and FIG. 3).

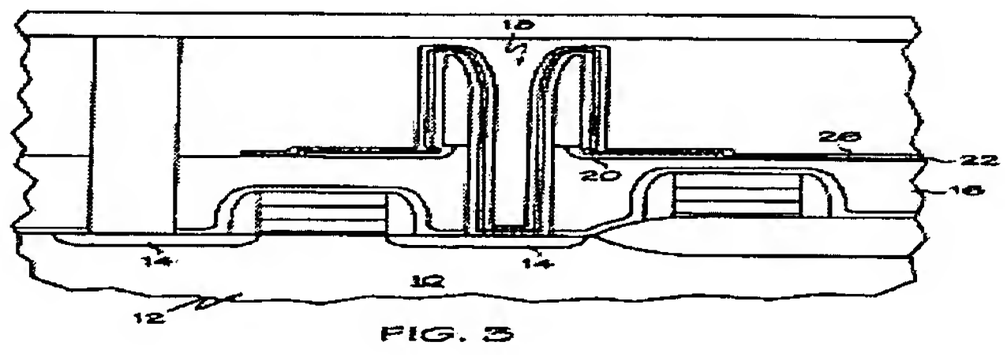

FIG. 3

In re claim 26, **Zheng** discloses that the formation of the conductive structure which electrically connects the first and second capacitor top plate portions comprises: etching the first and second capacitor top plate portions to form a sidewall comprising the first and second capacitor top plate portions; forming a blanket conductive layer on the sidewall; etching the blanket conductive layer to form a conductive spacer which contacts the sidewall and electrically connects the first and second capacitor top plate portions (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 27, **Zheng** discloses that the formation of the conductive structure which electrically connects the first and second capacitor top plate portions comprises: etching the first and second capacitor top plate portions to form an opening in the first and second capacitor top plate portions; and forming a conductive plug (unlabeled) within the opening in the first and second capacitor top plate portions (page 1, paragraphs [0012]- [0014] and FIGS. 1-2).

In re claim 28, **Zheng** discloses that the method of claim 25 further comprising : providing a semiconductor wafer substrate **12** assembly comprising a semiconductor wafer having a conductively-doped region therein; forming a

conductive pad to contact the conductively-doped region of the semiconductor wafer; during the formation of the first portion of the capacitor bottom plate **20**: forming a blanket conductive bottom plate layer; and spacer etching the blanket conductive bottom plate layer **20** to form the first portion of the capacitor bottom plate having an opening **18** therein whereby the conductive pad is exposed through the opening in a bottom of the bottom plate layer; and forming the second portion of the capacitor bottom plate to contact the first portion of the capacitor bottom plate layer and the conductive pad through the opening in the first portion of the bottom plate layer (page 1, paragraphs [0012]- [0014] and FIG. 2).

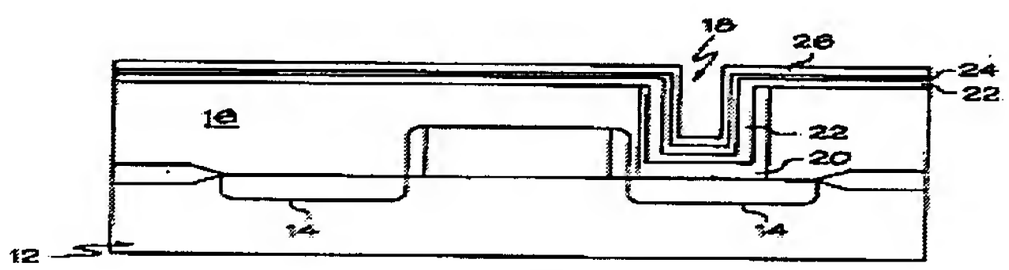

FIG. 2

Response to Applicants' Amendment and Arguments

Applicant's arguments filed July 22nd, 2005 have been fully considered but they are not persuasive.

Applicants contend that the reference Zheng et al. (U.S. Pub. 2003/0166318), herein known as Zheng fails to teach or suggest "forming a first conductive cross sectional spacer wherein…wherein the first conductive spacer forms a portion of a capacitor top late." Zheng either does not suggest a conductive spacer, or the conductive spacer is part of the bottom plate as discussed above. Zheng also does not teach or suggest forming a first capacitor cell dielectric layer on the first conductive spacer and "forming a second conductive cross sectional spacer on the first capacitor cell dielectric layer."

In response Applicants' contention that Zheng fails to teach or suggest "forming a first conductive cross sectional spacer wherein...wherein the first conductive spacer forms a portion of a capacitor top late." Zheng either does not suggest a conductive spacer, or the conductive spacer is part of the bottom plate as discussed above. Zheng also does not teach or suggest forming a first capacitor cell dielectric layer on the first conductive spacer and "forming a second conductive cross sectional spacer on the first capacitor cell dielectric layer", Examiner respectfully disagrees. Applicants are directed to (page 1, paragraph [0012] and FIG. 3) where Zheng discloses forming a first conductive cross-sectional spacer on the first dielectric sidewall wherein the first conductive spacer forms a portion of a capacitor top plate **20** (page 2, paragraph [0012]); forming a first capacitor cell dielectric layer **22** on the first conductive spacer **20**; and forming a second conductive cross-sectional spacer 26 on the first capacitor cell dielectric layer 22. Thus Zheng does teach Applicants' claimed invention.

For these reasons, examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the

date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
September 26th, 2005

W. David Coleman
Primary Examiner

OKAY TO ENTER
K.N.
09/26/05

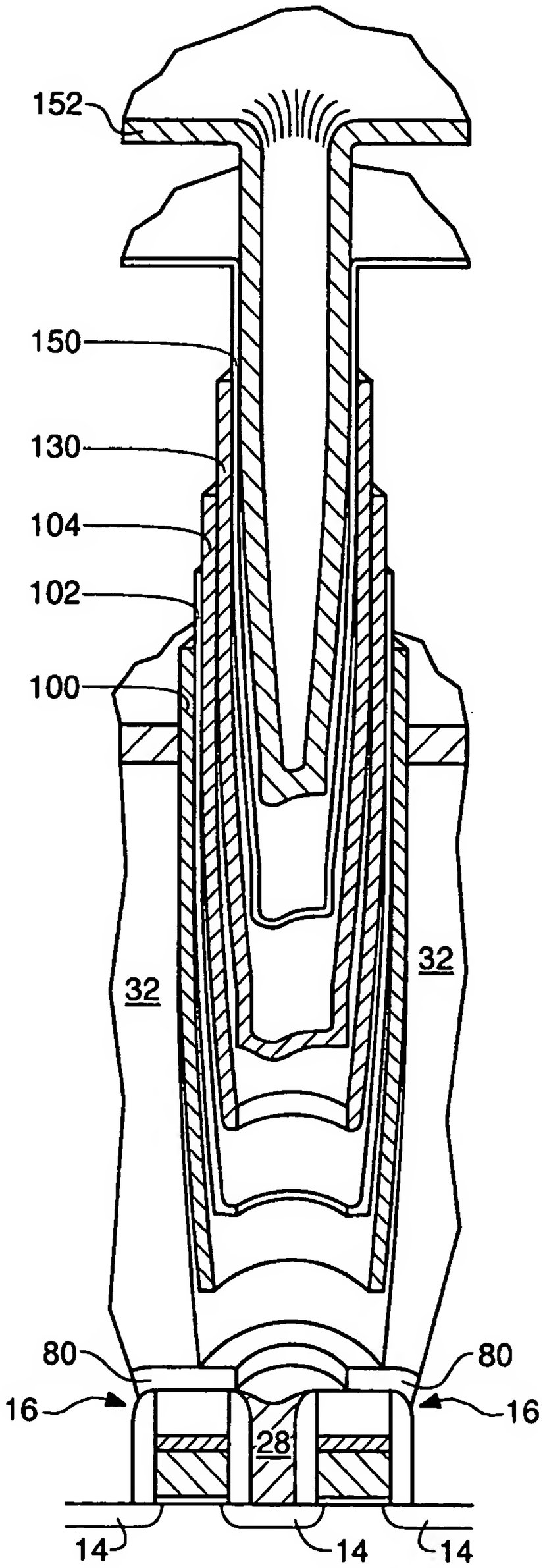

FIG. 22